



**Key Parameters**

$V_{DSM}$	= 6500V
$I_{T(AV)}$	= 1800A
$I_{TSM}$	= 47500A
$V_{T(TO)}$	= 1.20V
$r_T$	= 0.425mΩ

**Features**

- Double side cooling
- Full blocking capability over wide temperature range
- High surge current capability
- Hermetic metal case with ceramic insulator
- Low on-state and switching losses

**Applications**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

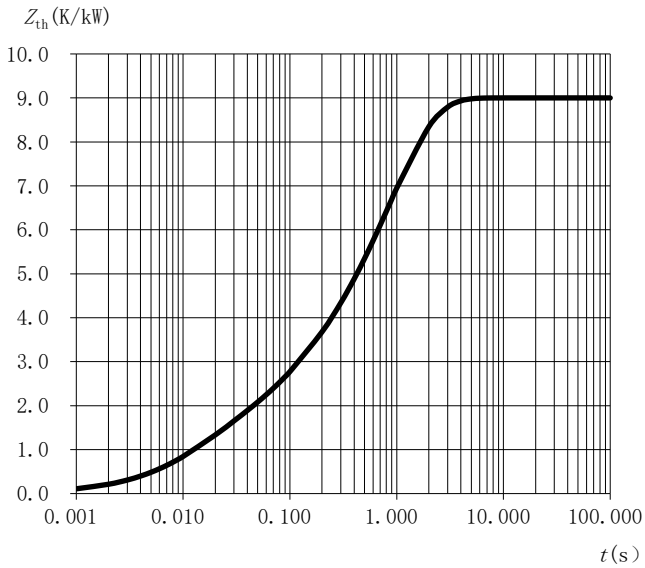
**Ordering Information**

MS PERI	T	1800	CZ	XX
Fixed Code	Phase Control Thyristor	Current Code	CZ - Capsule package with Free floating silicon Technology	$V_{DSM} \times 100$

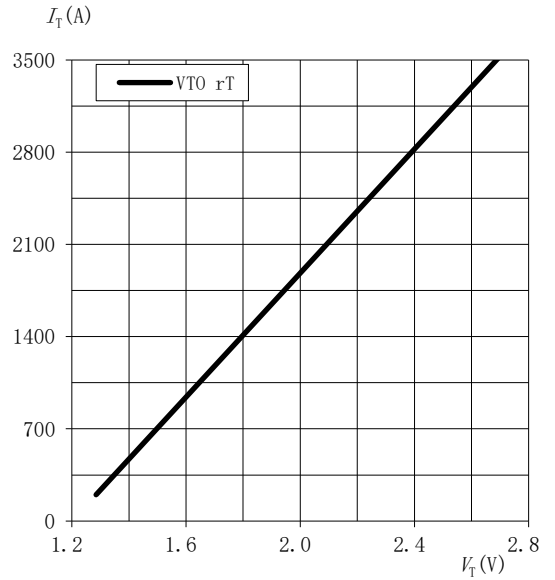
Order Code MS PERI T1800CZ65 : 6500V  $V_{DSM}$ , 35mm clamp height capsule thyristor

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Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>DSM</sub>	Maximum surge peak off-state voltage	f= 5Hz, t <sub>p</sub> =10msec	125	6500	V
V <sub>RSM</sub>	Maximum surge peak reverse voltage				
V <sub>DRM</sub>	Maximum repetitive peak off-state voltage	f= 50Hz, t <sub>p</sub> =10msec, t <sub>p1</sub> = 250μs 	125	6500	V
V <sub>RRM</sub>	Maximum repetitive peak reverse voltage				
V <sub>DWM</sub>	Maximum crest working forward voltage			4340	V
V <sub>RWM</sub>	Maximum crest working reverse voltage				
I <sub>RRM</sub>	Repetitive peak reverse current	V= V <sub>RRM</sub>	125	350	mA
I <sub>DRM</sub>	Repetitive peak off-state current	V= V <sub>DRM</sub>	125	350	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean on state current	180° sin ,50 Hz, T <sub>c</sub> =70°C, Double side cooled		1800	A
I <sub>RMS</sub>	RMS on-state current	T <sub>c</sub> =70°C, Double side cooled		2820	A
I <sub>TSM</sub>	Surge on-state current	Sine wave, 10 ms Without reverse voltage	125	47500	A
I <sup>2</sup> t	I <sup>2</sup> t		125	11281 x 10 <sup>3</sup>	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 1600A	125	1.88	V
V <sub>T(TO)</sub>	Threshold voltage		125	1.20	V
r <sub>T</sub>	On-state slope resistance		125	0.425	mΩ
I <sub>H</sub>	Holding current	V <sub>D</sub> =6V, gate open circuit	25	100	mA
I <sub>L</sub>	Latching current	V <sub>D</sub> =6V	25	1000	mA
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current		125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage	V <sub>DR</sub> = 67%V <sub>DRM</sub>	125	2000	V/μs
T <sub>q</sub>	Circuit commutated turn off time		125	800	μs
Q <sub>r</sub>	Recovered Charge		125	2800 - 3400	μC
<b>TRIGGERING</b>					
I <sub>GT</sub>	Gate trigger current	V <sub>D</sub> =6V	25	400	mA
V <sub>GT</sub>	Gate trigger voltage	V <sub>D</sub> =6V	25	2.60	V
I <sub>GD</sub>	Gate non-trigger current	V <sub>D</sub> =6V	125	10	mA
V <sub>GD</sub>	Gate non-trigger voltage	V <sub>D</sub> =6V	125	0.2	V
V <sub>FGM</sub>	Peak gate voltage (forward)			12	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			10	V
P <sub>GM</sub>	Peak gate power dissipation			See Fig. 7	W
P <sub>G(AV)</sub>	Average gate power dissipation			3	W
<b>THERMAL</b>					
R <sub>th(j-c)</sub>	Thermal impedance, sin 180°	Junction to case, Double side cooled		0.009	°C/W
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, Double side cooled		0.0015	°C/W
T <sub>j</sub>	Max. junction temperature			125	°C
T <sub>stg</sub>	Storage temperature			-40 .... 150	°C
<b>MECHANICAL</b>					
M	Clamping Force			63 - 84	kN
W	Weight (Approx.)			2000	gm
D <sub>s</sub>	Surface creepage distance			45	mm
D <sub>a</sub>	Air strike distance			21	mm
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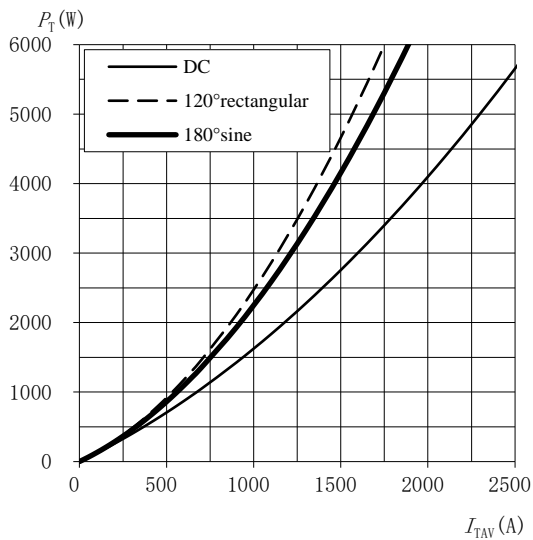
**Fig.1 : Transient thermal impedance (junction-to-case) vs. time**



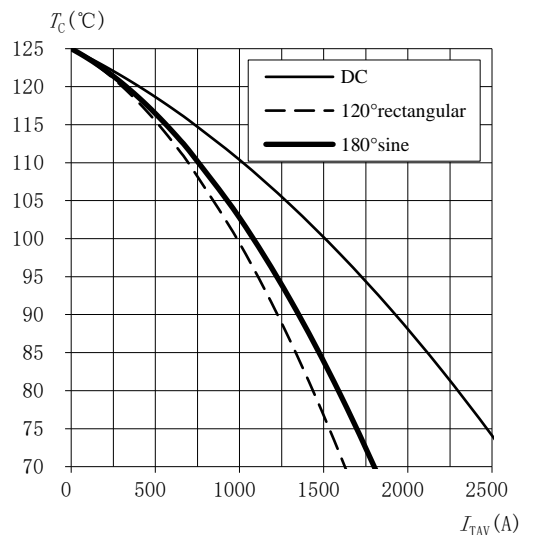
**Fig.2 : On-state V-I characteristics**

$$Z_{th(j-c)}(t) = \sum_{i=1}^n R_i(1 - e^{-t/\tau_i})$$

<i>i</i>	1	2	3	4
$R_i$ (K/kW)	6.4200	0.7900	1.0700	0.7200
$\tau_i$ (s)	0.8775	0.1423	0.0124	0.0525

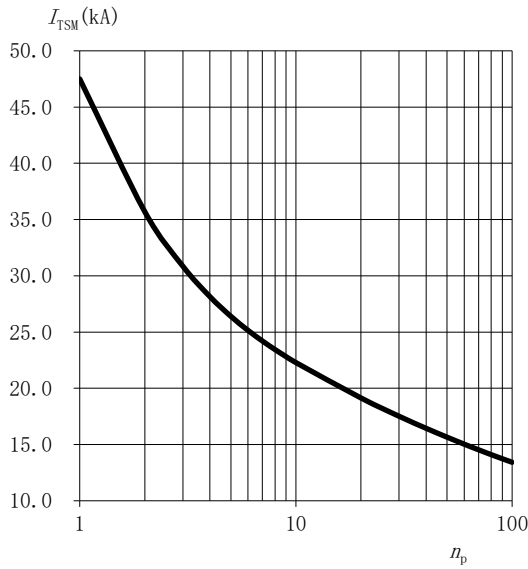


**Fig.3 : On-state power loss ( $P_T$ ) vs. average on-state Current ( $I_{TAV}$ )**

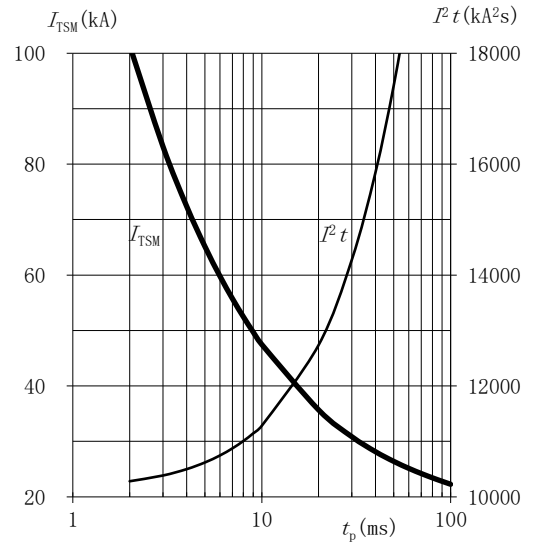


**Fig.4 : Max. permissible case temperature( $T_c$ ) vs. average on-state current( $I_{TAV}$ )**

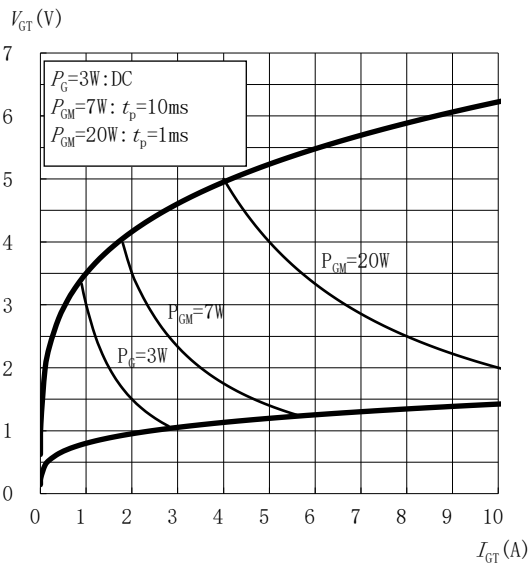
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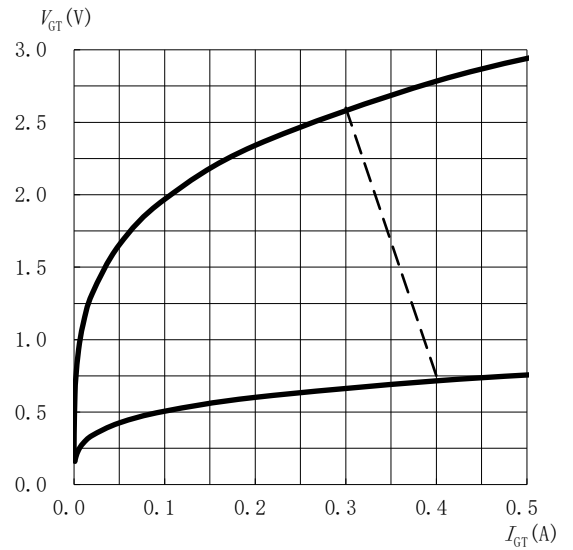
**Fig.5: Surge on-state current ( $I_{TSM}$ ) vs. number of pulses ( $n_p$ )**



**Fig.6: Surge on-state current ( $I_{TSM}$ ) and surge current Integral ( $I^2 t$ ) vs. pulse length ( $t_p$ )**



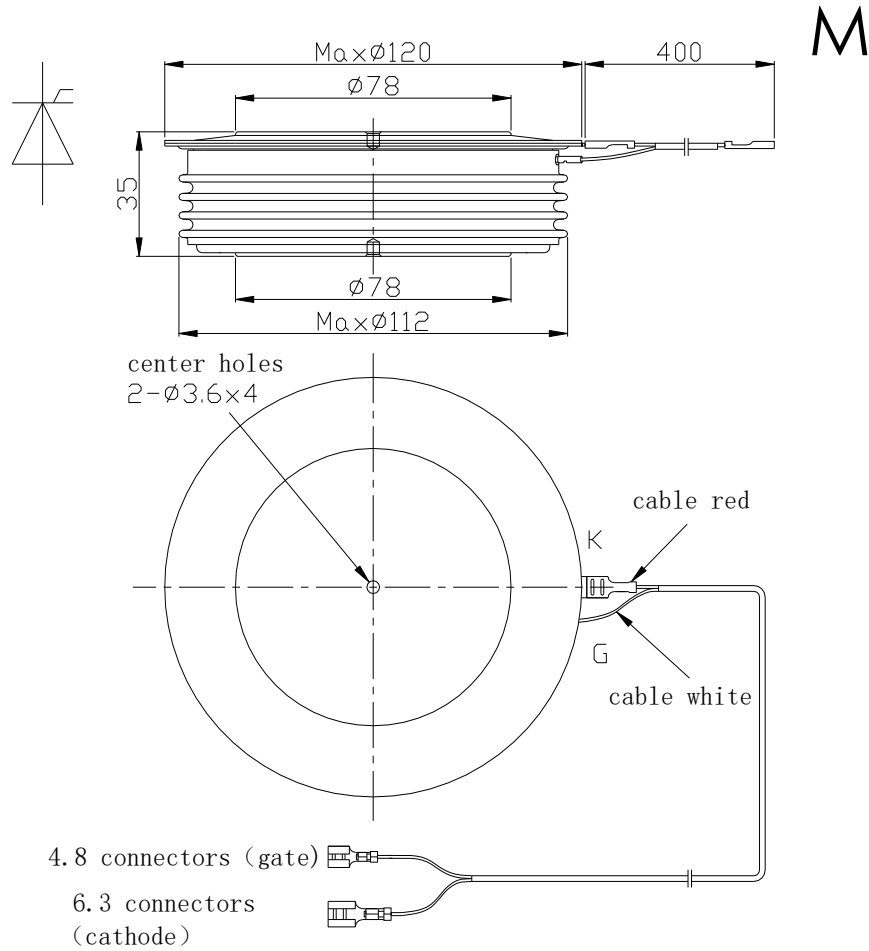
**Fig.7: Max. peak gate power loss**



**Fig.8: Gate trigger characteristics**

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