



Key Parameters

V_{DSM}	= 6500V
$I_{T(AV)}$	= 860A
I_{TSM}	= 15100A
$V_{T(TO)}$	= 1.20V
r_T	= 1.050mΩ

Features

- Double side cooling
- Full blocking capability over wide temperature range
- High surge current capability
- Hermetic metal case with ceramic insulator
- Low on-state and switching losses

Applications

- High Power Drives
- High Voltage Power Supplies
- Static Switches

Ordering Information

MS PERI	T	860	CZ	XX
Fixed Code	Phase Control Thyristor	Current Code	CZ - Capsule package with Free floating silicon Technology	$V_{DSM} \times 100$

Order Code MS PERI T860CZ65 : 6500V V_{DSM} , 26mm clamp height capsule thyristor

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Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit
BLOCKING					
V _{DSM}	Maximum surge peak off-state voltage	f= 5Hz, t _p =10msec	125	6500	V
V _{RSM}	Maximum surge peak reverse voltage				
V _{DRM}	Maximum repetitive peak off-state voltage	f= 50Hz, t _p =10msec, t _{p1} = 250μs 	125	6500	V
V _{RRM}	Maximum repetitive peak reverse voltage				
V _{DWM}	Maximum crest working forward voltage				
V _{RWM}	Maximum crest working reverse voltage				
I _{RRM}	Repetitive peak reverse current				
I _{DRM}	Repetitive peak off-state current	V= V _{DRM}	125	200	mA
CONDUCTING					
I _{T(AV)}	Mean on state current	180° sin ,50 Hz, T _c =70°C, Double side cooled		860	A
I _{RMS}	RMS on-state current	T _c =70°C, Double side cooled		1350	A
I _{TSM}	Surge on-state current	Sine wave, 10 ms Without reverse voltage	125	15100	A
I ² t	I ² t		125	1140 x 10 ³	A ² s
V _T	On-state voltage	On-state current = 1000A	125	2.25	V
V _{T(TO)}	Threshold voltage		125	1.20	V
r _T	On-state slope resistance		125	1.050	mΩ
I _H	Holding current	V _D =6V, gate open circuit	25	100	mA
I _L	Latching current	V _D =6V	25	1000	mA
SWITCHING					
di/dt	Critical rate of rise of on-state current		125	150	A/μs
dv/dt	Critical rate of rise of off-state voltage	V _{DR} = 67%V _{DRM}	125	2000	V/μs
T _q	Circuit commutated turn off time		125	1000	μs
Q _r	Recovered Charge		125	2250 - 2750	μC
TRIGGERING					
I _{GT}	Gate trigger current	V _D =6V	25	400	mA
V _{GT}	Gate trigger voltage	V _D =6V	25	2.60	V
I _{GD}	Gate non-trigger current	V _D =6V	125	10	mA
V _{GD}	Gate non-trigger voltage	V _D =6V	125	0.2	V
V _{FGM}	Peak gate voltage (forward)			12	V
I _{FGM}	Peak gate current			10	A
V _{RGM}	Peak gate voltage (reverse)			10	V
P _{GM}	Peak gate power dissipation			See Fig. 7	W
P _{G(AV)}	Average gate power dissipation			3	W
THERMAL					
R _{th(j-c)}	Thermal impedance, sin 180°	Junction to case, Double side cooled		0.017	°C/W
R _{th(c-h)}	Thermal impedance	Case to heatsink, Double side cooled		0.004	°C/W
T _j	Max. junction temperature			125	°C
T _{stg}	Storage temperature			-40 150	°C
MECHANICAL					
M	Clamping Force			18 - 26	kN
W	Weight (Approx.)			500	gm
D _s	Surface creepage distance			25	mm
D _a	Air strike distance			14	mm
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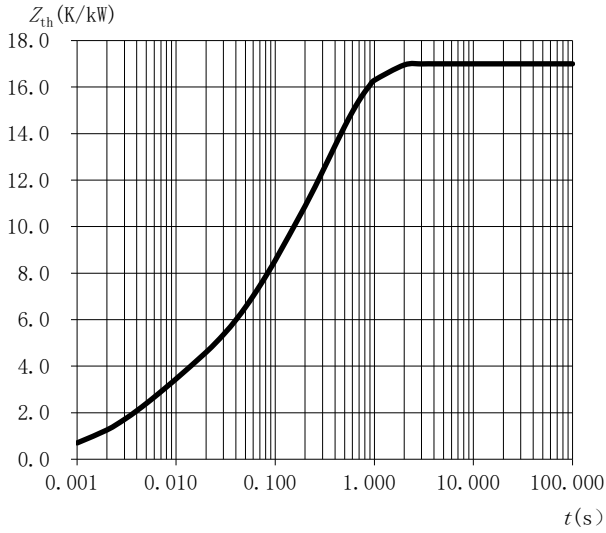


Fig.1 : Transient thermal impedance (junction-to-case) vs. time

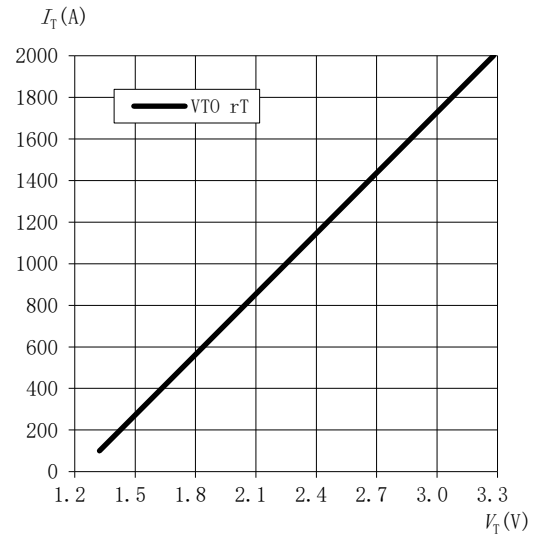


Fig.2 : On-state V-I characteristics

$$Z_{th(j-c)}(t) = \sum_{i=1}^n R_i(1 - e^{-t/\tau_i})$$

<i>i</i>	1	2	3	4
<i>R_i</i> (K/kW)	10.31	2.1	3.74	0.85
<i>τ_i</i> (s)	0.3733	0.006	0.0526	0.0025

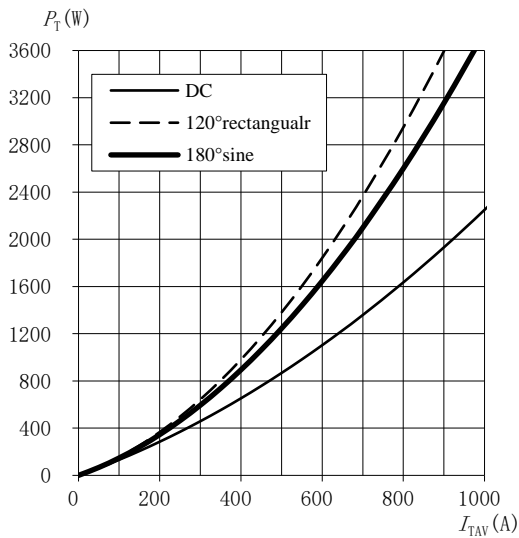


Fig. 3 : On-state power loss (*P_T*) vs. average on-state Current (*I_{TAV}*)

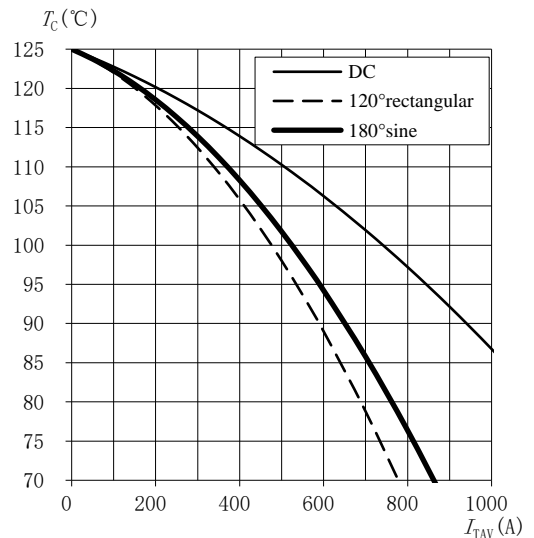


Fig.4 : Max. permissible case temperature(*T_c*) vs. average on-state current(*I_{TAV}*)

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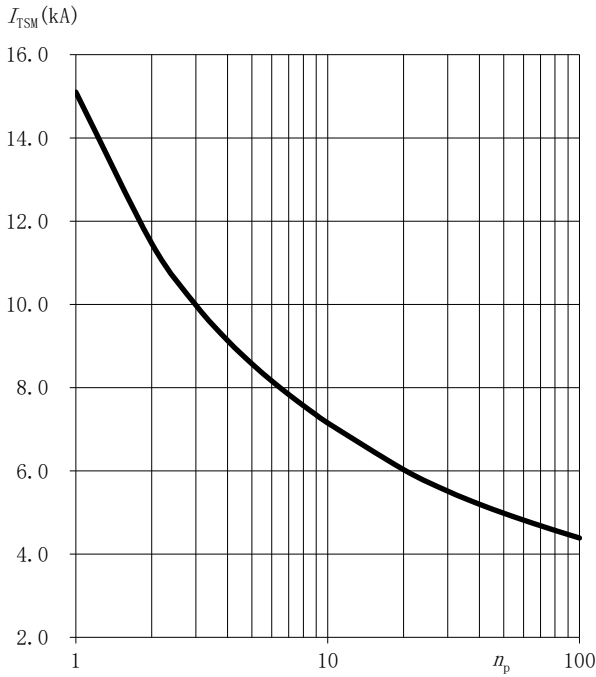


Fig.5: Surge on-state current (I_{TSM}) vs. number of pulses (n_p)

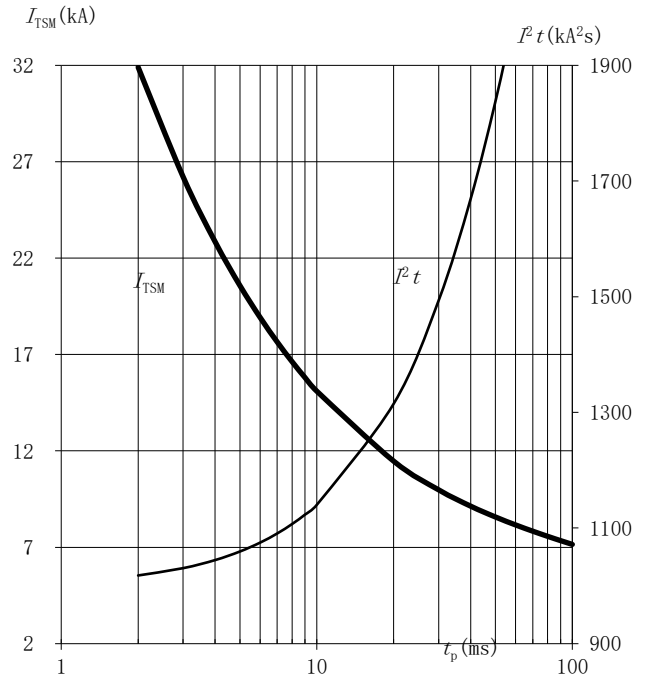


Fig.6: Surge on-state current (I_{TSM}) and surge current Integral ($I^2 t$) vs. pulse length (t_p)

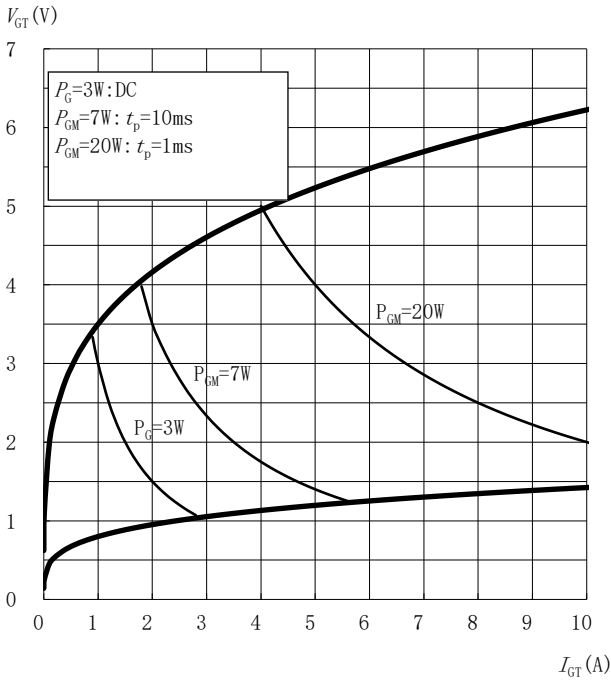


Fig.7: Max. peak gate power loss

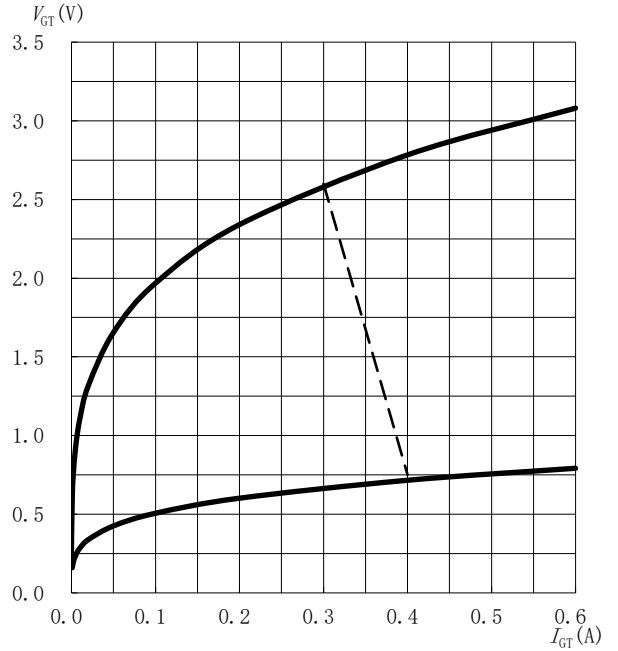
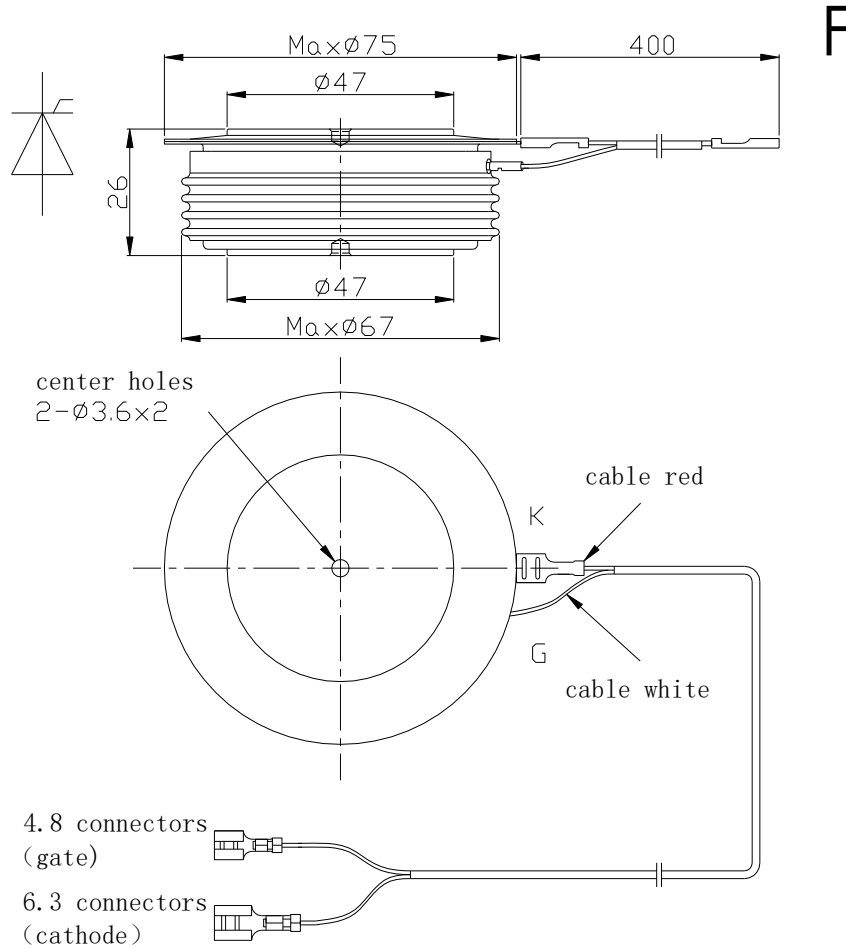


Fig.8: Gate trigger characteristics

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