In association with

MS PERI TF4068CZ28

Technical Information

Fast Switching Thyristor

Key Parameters

V_{DRM}/ V_{RRM}	= 2800V
$I_{T(AV)}$	= 4068A
I_{TSM}	= 61155A
$V_{T(TO)}$	= 1.14V
r_T	= 0.16mΩ
T_q	= 85µsec

Features

- Double side cooling
- Full blocking capability over wide temperature range
- High surge current capability
- Hermetic metal case with ceramic insulator
- Low on-state and switching losses

Applications

- High Power Drives
- High Voltage Power Supplies
- Static Switches
- Motor control
- Transportation
- Induction Heating

Ordering Information

MS PERI	TF	4068	CZ	X X
Fixed Code	Fast Switching Thyristor	Current Code	CZ - Capsule package with Free floating silicon Technology	Voltage Code Code X 100 = V_{DRM}/V_{RRM}
Order Code MS PERI TF4068CZ25 : 2500V V_{DRM}/V_{RRM}, 35mm clamp height capsule thyristor				

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Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{DSM}	Maximum non-repetitive peak off-state voltage	f= 5Hz, t_p=10msec	125	3000	V
V_{RSM}	Maximum non-repetitive peak reverse voltage				
V_{DRM}	Maximum repetitive peak off-state voltage	f= 50Hz, t_p=10msec	125	2800	V
V_{RRM}	Maximum repetitive peak reverse voltage				
I_{RRM}	Repetitive peak reverse current	V= V_{RRM}	125	300	mA
I_{DRM}	Repetitive peak off-state current	V= V_{DRM}	125	300	mA
CONDUCTING					
$I_{T(AV)}$	Mean on state current	180° sin ,50 Hz, T_c=55°C, Double side cooled		4068	A
I_{RMS}	RMS on-state current	T_c=55°C, Double side cooled		6400	A
I_{TSM}	Surge on-state current	Sine wave, 10 ms Without reverse voltage	125	61155	A
I^2t	I^2t		125	18700×10^3	A^2s
V_T	On-state voltage	On-state current = 6000A	125	2.10	V
$V_{T(TO)}$	Threshold voltage		125	1.14	V
r_T	On-state slope resistance		125	0.16	mΩ
I_H	Holding current	V_D=6V, gate open circuit	25	200	mA
I_L	Latching current	V_D=6V	25	1000	mA
SWITCHING					
di/dt	Critical rate of rise of on-state current		125	200	A/µs
dv/dt	Critical rate of rise of off-state voltage	V_{DR} = 67%V_{DRM}	125	1000	V/µs
Tq	Circuit commutated turn off time	I_{TM}=2000A, -di_F /dt = 60A/µs, V_R =100V,t_p=4000µs Reapplied dv/dt = 200V/µs, V_{DR} = 800V	125	85	µs
Q_r	Recovered Charge	I_{TM}=2000A, -di_F /dt =60A/µs, V_R = 100V,t_p=4000 µs	125	1900 - 2200	µC
TRIGGERING					
I_{GT}	Gate trigger current	V_D=6V	25	400	mA
V_{GT}	Gate trigger voltage	V_D=6V	25	2.60	V
I_{GD}	Gate non-trigger current	V_D=6V	125	10	mA
V_{GD}	Gate non-trigger voltage	V_D=6V	125	0.2	V
V_{FGM}	Peak gate voltage (forward)			12	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			10	V
P_{GM}	Peak gate power dissipation			See Fig. 7	W
$P_{G(AV)}$	Average gate power dissipation			3	W
THERMAL					
R th(j-c)	Thermal impedance, sin 180°	Junction to case, Double side cooled		0.0057	°C/W
R th(c-h)	Thermal impedance	Case to heatsink, Double side cooled		0.001	°C/W
T j	Max. junction temperature			125	°C
T stg	Storage temperature			-40 150	°C
MECHANICAL					
M	Clamping Force			81 - 108	kN
W	Weight (Approx.)			2900	gm
D_S	Surface creepage distance			56	mm
D_a	Air strike distance			22	mm

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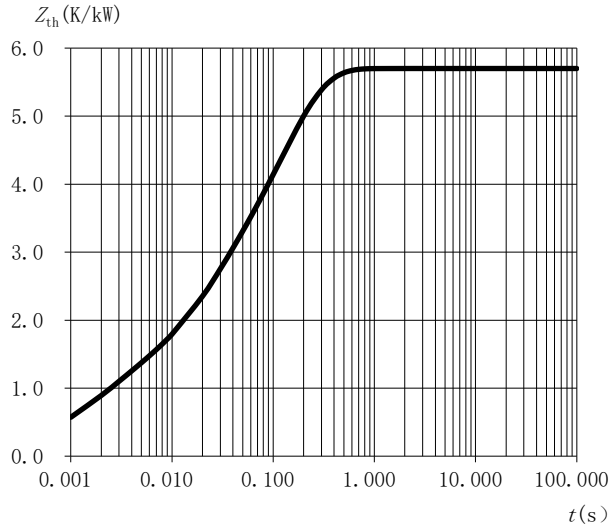

Fig.1 : Transient thermal impedance (junction-to-case) vs. time

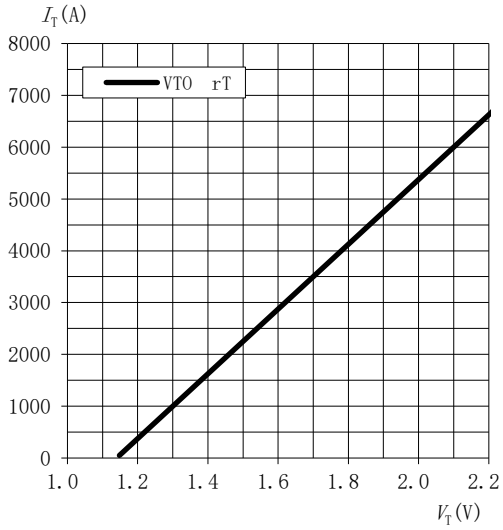

Fig.2 : On-state V-I characteristics

$$Z_{th(j\text{-}c)}(t) = \sum_{i=1}^{n} R_i(1-e^{-t/\tau_i})$$

i	1	2	3	4
R_i(K/kW)	4.347	1.129	0.859	0.663
τ_i(s)	1.029	0.188	0.012	0.065

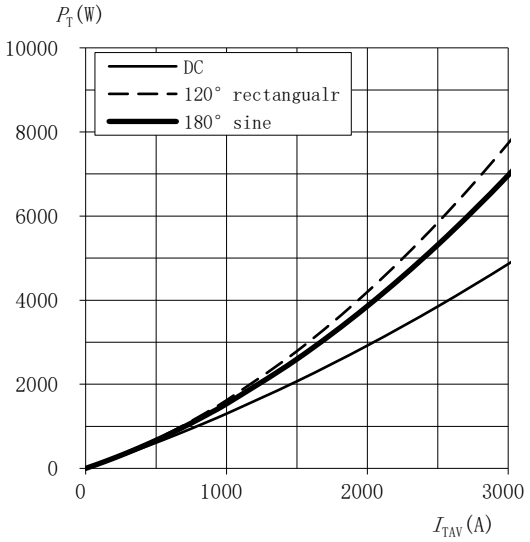

Fig. 3 : On-state power loss (P_T) vs. average on-state Current (I_{TAV})

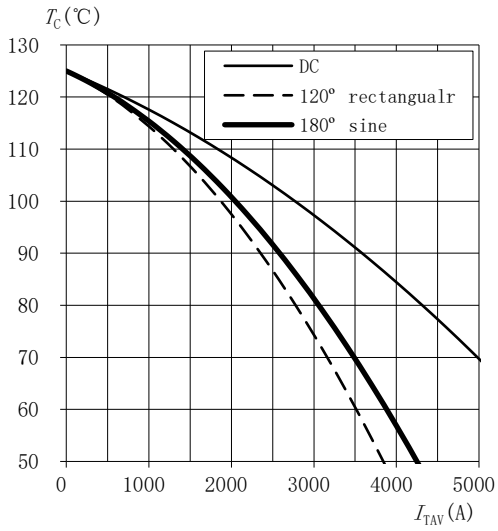

Fig.4 : Max. permissible case temperature(T_C) vs. average on-state current(I_{TAV})

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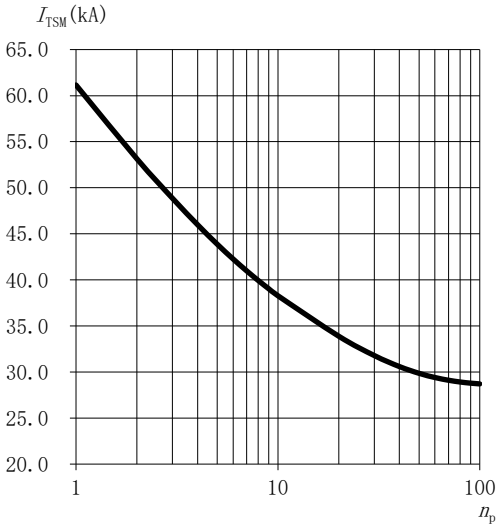

Fig.5: Surge on-state current (I_{TSM}) vs. number of pulses (n_p)

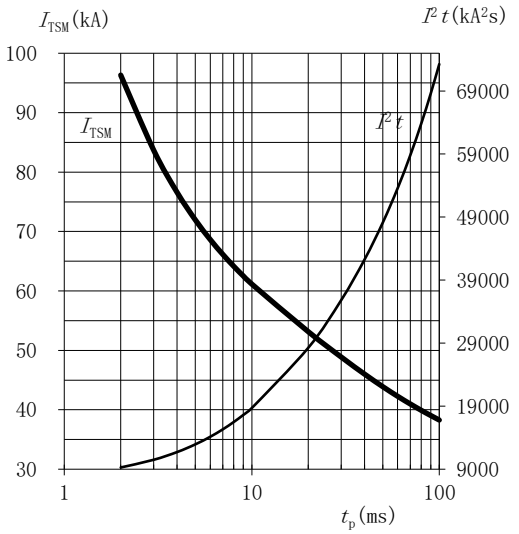

Fig.6: Surge on-state current (I_{TSM}) and surge current Integral (I^2t) vs. pulse length (t_p)

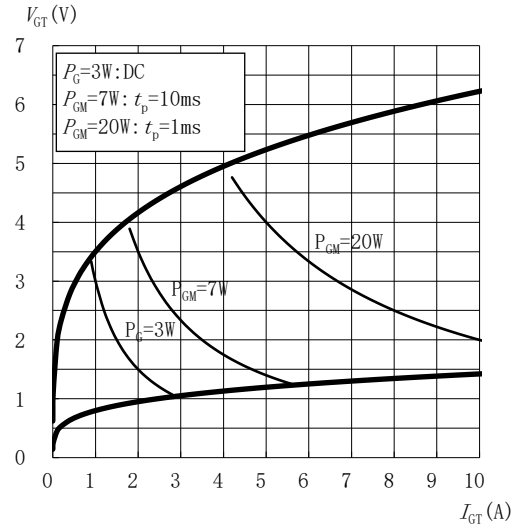

Fig.7: Max. peak gate power loss

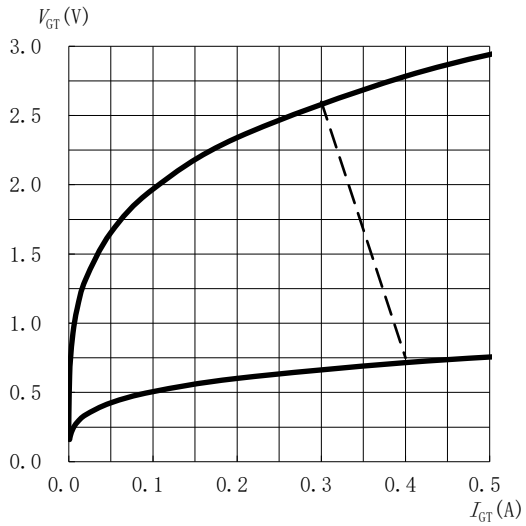

Fig.8: Gate trigger characteristics

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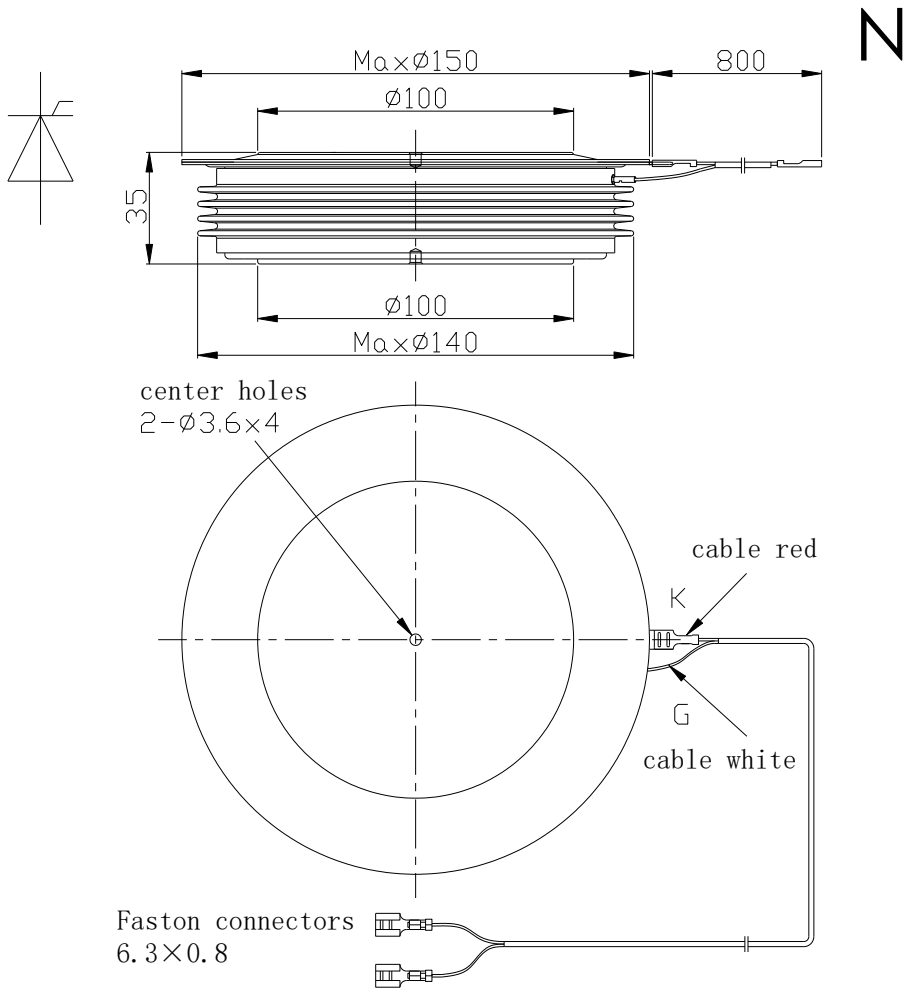
Outline :



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