



**Key Parameters**

$V_{DRM} / V_{RRM}$	= 3000V
$I_{T(AV)}$	= 1470A
$I_{TSM}$	= 24kA
$V_{T(TO)}$	= 0.97V
$r_T$	= 0.27m $\Omega$

**Features**

- Full blocking capability over wide temperature range
- High Surge current capability
- Hermetic metal case with ceramic insulator

**Applications**

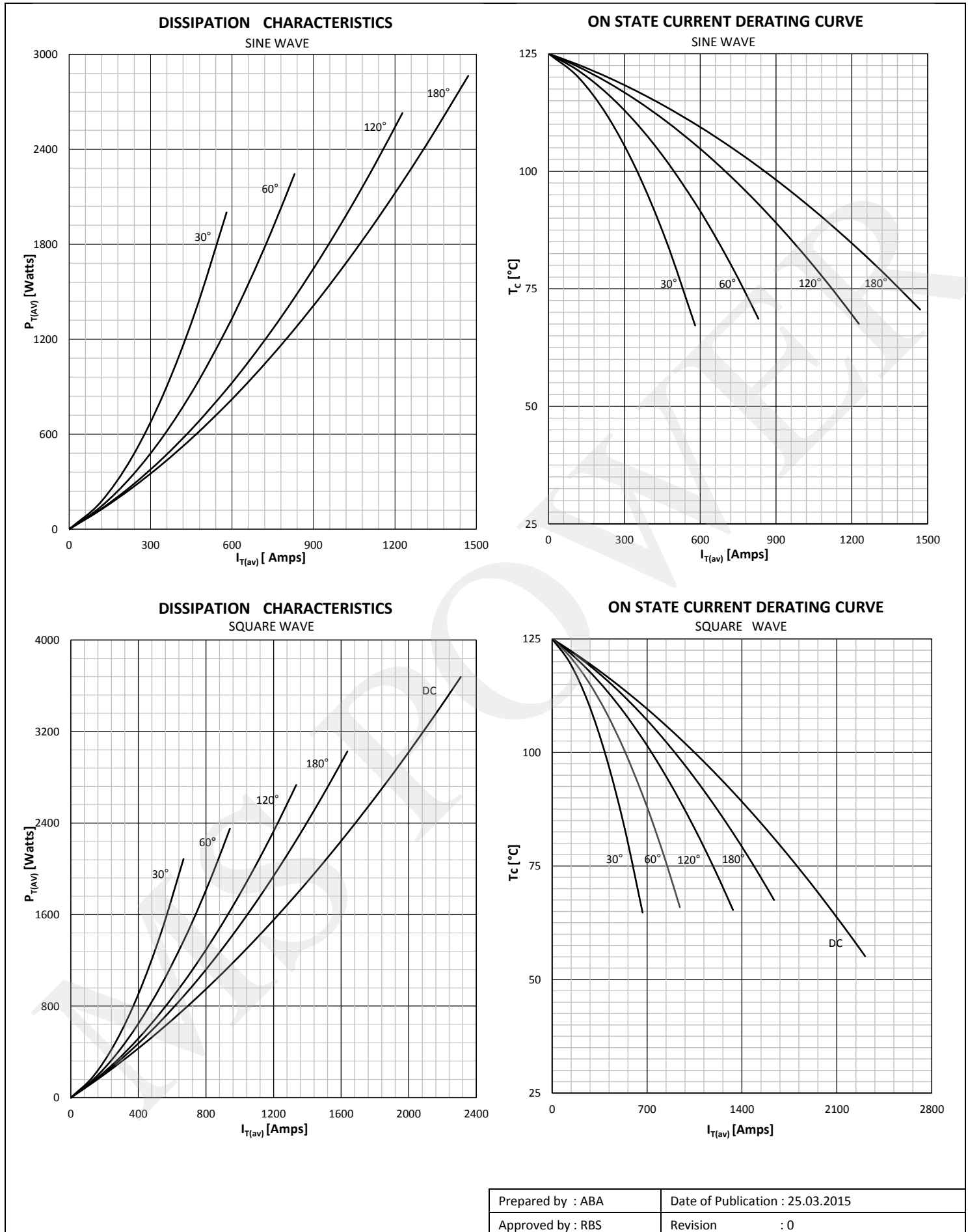
- Battery Chargers
- Medical Equipment
- UPS
- Power Supplies
- Motor control
- Controlled Rectifiers
- Transportation
- Induction Heating
- Welding

**Ordering Information**

MS T	1470	C	XX
Phase Control Thyristor	Current Code	C - Capsule package with Alloyed silicon technology	Voltage Code Code X 100 = $V_{DRM}/V_{RRM}$
Order Code MS T1470C30 : 3000V $V_{DRM}, V_{RRM}$ , 26mm clamp height capsule thyristor			

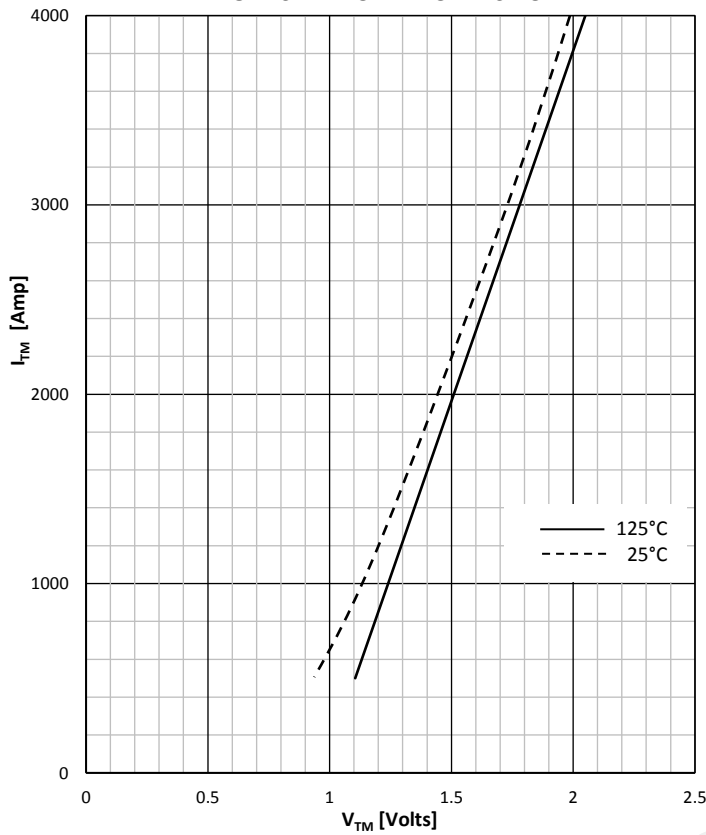
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Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM</sub>	Repetitive peak reverse voltage		125	2000 - 3000	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		125	2100 - 3100	V
V <sub>DRM</sub>	Repetitive peak off-state voltage		125	2000 - 3000	V
I <sub>RRM</sub>	Repetitive peak reverse current	V = V <sub>RRM</sub>	125	100	mA
I <sub>DRM</sub>	Repetitive peak off-state current	V = V <sub>DRM</sub>	125	100	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean on state current	180° sin ,50 Hz, T <sub>c</sub> =70°C, Double side cooled 180° sin ,50 Hz, T <sub>c</sub> =72°C, Double side cooled		1470 1440	A
I <sub>RMS</sub>	RMS on-state current	T <sub>c</sub> =70°C, Double side cooled		2308	A
I <sub>TSM</sub>	Surge on-state current	Sine wave, 10 ms Without reverse voltage	25	24000	A
			125	23000	A
I <sup>2</sup> t	I <sup>2</sup> t	Sine wave, 10 ms Without reverse voltage	25	2880 x 10 <sup>3</sup>	A <sup>2</sup> s
			125	2645 x 10 <sup>3</sup>	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 3000A	125	1.78	V
V <sub>T(TO)</sub>	Threshold voltage		125	0.97	V
r <sub>T</sub>	On-state slope resistance		125	0.27	mΩ
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current		125	150	A/μs
dv/dt	Critical rate of rise of off-state voltage	V <sub>DR</sub> = 67%V <sub>DRM</sub>	125	1000	V/μs
<b>GATE</b>					
I <sub>gt</sub>	Gate trigger current	V <sub>D</sub> =6V	25	300	mA
V <sub>gt</sub>	Gate trigger voltage	V <sub>D</sub> =6V	25	3.0	V
I <sub>H</sub>	Holding current	V <sub>D</sub> =6V, gate open circuit	25	800	mA
I <sub>L</sub>	Latching current	V <sub>D</sub> =6V	25	1000	mA
<b>MOUNTING</b>					
R <sub>th(j-c)</sub>	Thermal impedance, sin 180°	Junction to case, Double side cooled		0.019	°C/W
R <sub>th(j-c)</sub>	Thermal impedance, rec120°	Junction to case, Double side cooled		0.022	°C/W
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, Double side cooled		0.004	°C/W
T <sub>j</sub>	Max. junction temperature			125	°C
T <sub>stg</sub>	Storage temperature			-40 ... 125	°C
M	Clamping Force			22 - 26	kN
W	Weight (Approx.)			510	gm
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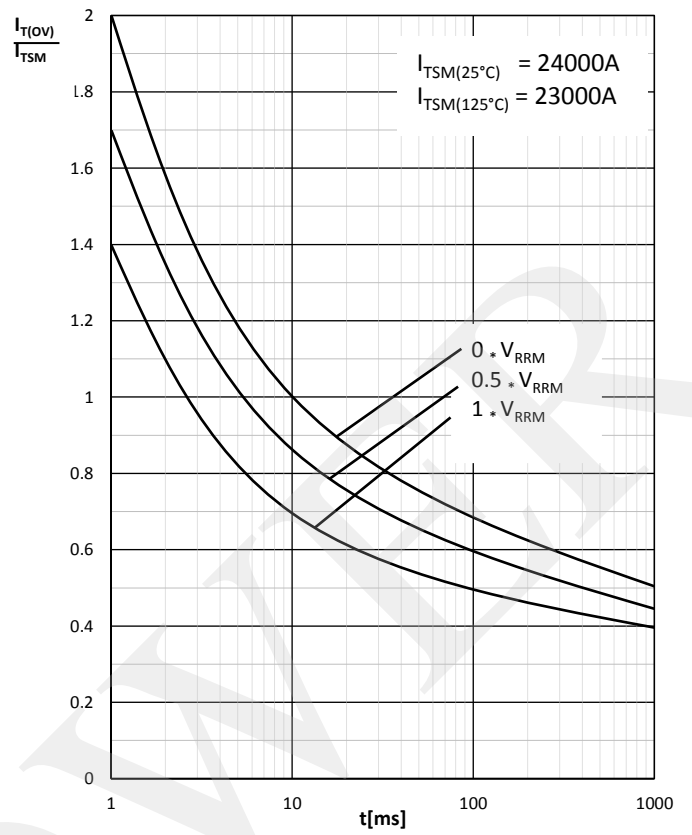


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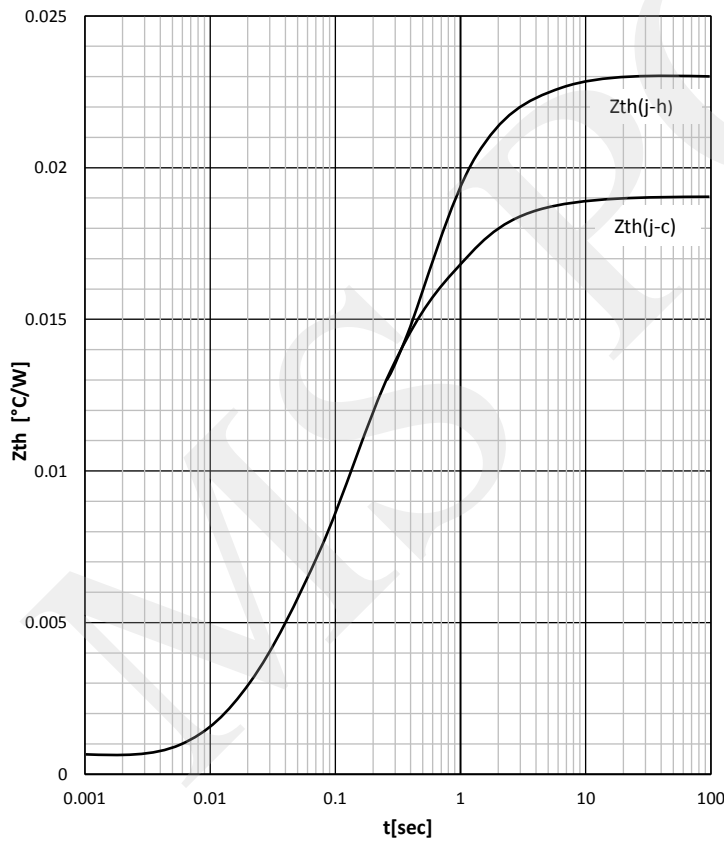
ON -STATE CHARACTERISTIC



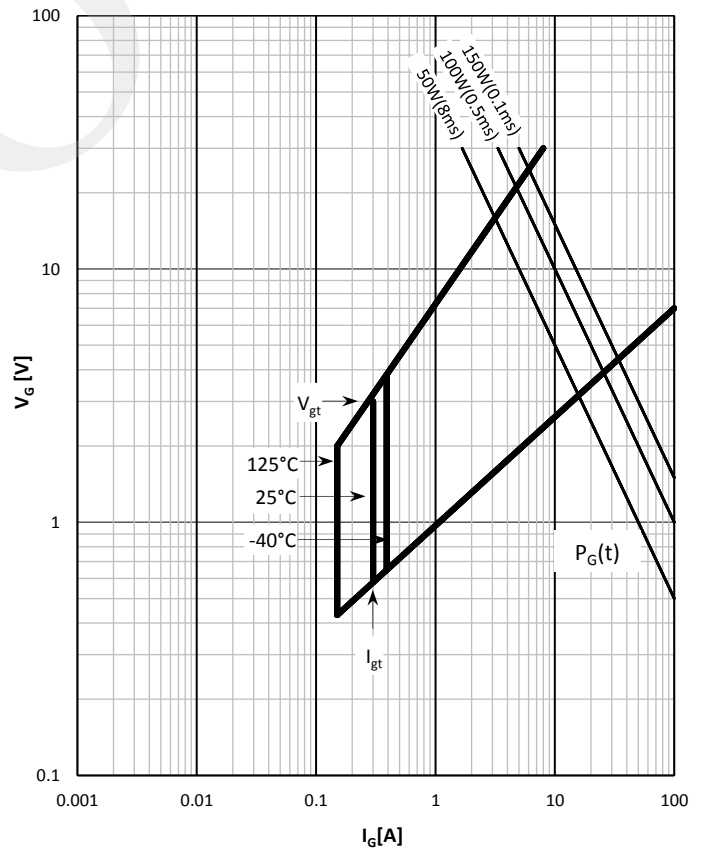
SURGE CHARACTERISTICS



TRANSIENT THERMAL IMPEDANCE, PER ARM



GATE TRIGGER CHARACTERISTICS



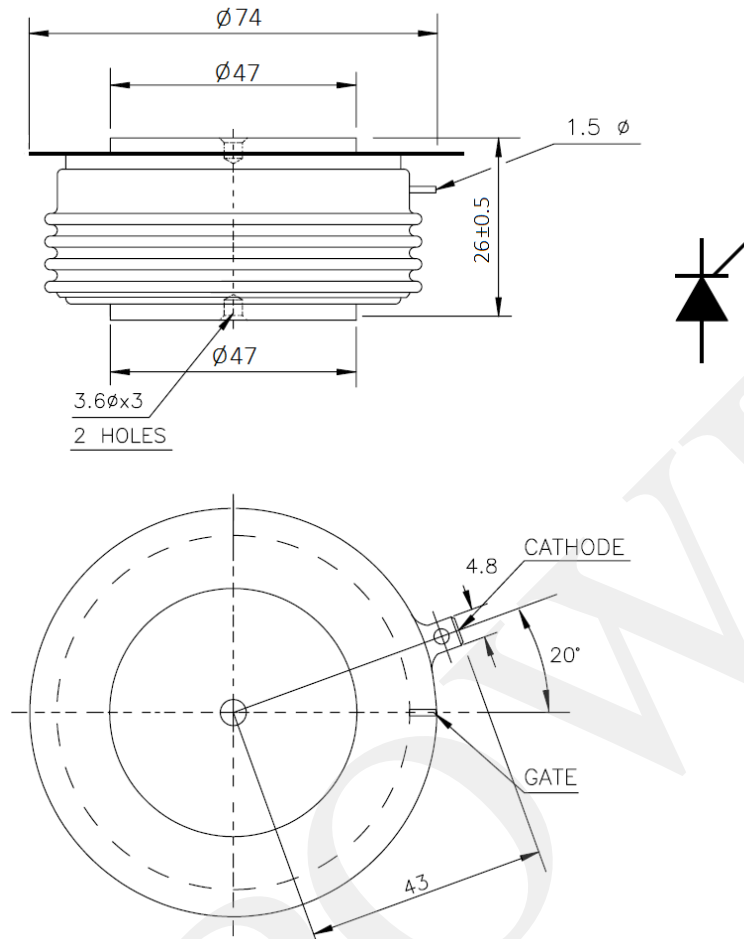
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Outline



**MS Power GmbH**

Mergenthalerallee 79-81  
65760 Eschborn, Germany  
Web: [www.mspowergroup.com](http://www.mspowergroup.com)  
Mail: [info@mspowergroup.de](mailto:info@mspowergroup.de)

**Sales & Enquiry:**

[sales@mspowergroup.de](mailto:sales@mspowergroup.de)

**Technical Support:**

[solution@mspowergroup.de](mailto:solution@mspowergroup.de)

**After sales Service:**

[service@mspowergroup.de](mailto:service@mspowergroup.de)

Phone: +49 (0) 6196/7768 666

Fax: +49 (0) 6196/7757 888



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